LOW NOISE DATA CONVERSION CIRCUITS
AND METHODS AND SYSTEMS USING THE SAME

FIELD OF THE INVENTION

[0001]   The present invention relates in general to mixed – signal circuits and methods and in particular to low - noise data conversion circuits and methods and systems using the same.

BACKGROUND OF INVENTION

[0002]   Noise and harmonic distortion in mixed-signal circuitry, such as digital to analog and analog to digital converters (DACs and ADCs), comes from a number of sources. For example, the voltages at the summing nodes in some operational amplifier circuits do not completely settle after switching operations, resulting in high frequency noise on the corresponding signal lines. This high frequency noise is then sampled onto the parasitic capacitance within the circuitry and subsequently folded-back into the signal baseband during later switching operations. Unacceptable noise and distortion can also be the result of an inadequate power supply rejection ratio (PSRR) within the various circuits and current "kicks" on the signal lines caused by the switching of unbalanced loads.

[0003]   In noise sensitive applications, including audio processing, the minimization of distortion and noise are critical design factors, since often their ultimate effect is perceptible to the end-user. However, designing to minimize noise and harmonic distortion presents significant challenges, especially when other design factors must be considered, such as circuit complexity, chip area, and power consumption.

SUMMARY OF INVENTION

[0004]   The principles of the present invention generally provide noise reduction techniques suitable for applications such as data converters with significant out of band noise and similar circuitry. According to one particular embodiment of these principles, a circuit is disclosed including a first element sampling noise from and discharging noise to a signal line in response to an input signal transitioning on selected edges of a clock signal. A second element samples noise from and discharges noise to the signal line in response to another input signal transitioning on other edges of the clock signal differing from the selected edges of the clock signal such that the sampling and discharging frequency on the signal line is independent on the of the input signal and the other input signal.

[0005]   In another embodiment of the inventive principles, a data conversion element selectively switches a parasitic capacitance to the signal line in response to the input signal. An associated dummy circuit switches a matching parasitic capacitance to the signal line in response to the complement of the input signal.

[0006]   In a further embodiment of the inventive principles, a dummy conversion element selectively switches a parasitic capacitance to the signal line in response to the another input signal. A dummy circuit switches a matching parasitic capacitance to the signal line in response to the complement of the another input signal.

[0007]   By utilizing a dummy conversion element, which switches a matching load to the signal line on clock edges differing from the clock edges timing the switching of the load of the data conversion element to the signal line, the sampling transitions due to parasitic capacitance become independent of the input signal. The mixing of high frequencies on the signal lines due to sampling is more controlled, such that fold back of noise into the signal baseband can be minimized.

[0008]   Switching a parasitic capacitance, matched to the parasitic capacitance of the data conversion element to the signal line in response to the complement of the

input signal improves the power supply rejection ratio, lowers the differential "kick" on the signal line, and makes the load on the signal line independent of the input data. A similar technique is advantageously applied to the dummy conversion element using the complement of the other input signal.

BRIEF DESCRIPTION OF DRAWINGS

[0009]   For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010]   FIGURE 1 is a diagram of a typical audio system suitable for describing the utilization of a digital-to-analog converter subsystem (DAC) according to the principles of the present invention;

[0011]   FIGURE 2 is an electrical schematic diagram of an exemplary DAC subsystem embodying the principles of the present invention;

[0012]   FIGURE 3A is a more detailed block diagram of the current DAC shown in FIGURE 2;

[0013]   FIGURE 3B is a timing diagram of exemplary signals controlling the operation of the current DAC shown in FIGURES 2 and 3A;

[0014]   FIGURE 4A is an electrical schematic illustrating in further detail a digital to analog conversion element of the current-based DAC array shown in FIGURE 3A and associated level – shifting circuitry;

[0015]   FIGURE 4B is an electrical schematic diagram of exemplary control signal generation circuitry suitable for generating the chopping control signals shown in FIGURE 3A; and

[0016]   FIGURE 5 is an electrical schematic diagram of an exemplary dummy element shown in FIGURE 3A.

DETAILED DESCRIPTION OF THE INVENTION

[0017]   The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURE 1- 5 of the drawings, in which like numbers designate like parts.

[0018]   FIGURE 1 is a diagram of a typical audio system 100 suitable for describing the utilization of a digital-to-analog converter subsystem (DAC) 101 according to the principles of the present invention. In this example, DAC subsystem 101 forms part of an audio component 102, such as a compact disk (CD) player, digital audio tape (DAT) player, or digital versatile disk (DVD) unit. A digital media drive 103 recovers the digital data from the given storage media and passes those data, along with clocks and control signals, to DAC subsystem 101. The resulting analog (audio) signal undergoes further processing in analog/audio processing block 104 prior to amplification in audio amplification block 105. Audio amplification block 105 then drives a set of conventional speakers 106a and 106b, or a headset (not shown).

[0019]   Multi-bit digital audio data is received by DAC subsystem 100 serially through the SDATA pin timed by the serial clock (SCLK) signal. The left and right channel data are alternately processed in response to the left-right clock (LRCK) signal, which is normally at the sampling rate. In system 100, the external master clock (EMCK) signal is received by DAC subsystem 101 from digital media drive 103.

[0020]   FIGURE 2 is a block diagram of a digital to analog converter (DAC) 200 embodying the principles of the present invention, and which forms a portion of DAC subsystem 101 of FIGURE 1. In the illustrated embodiment, DAC 200 receives a channel of digital audio data AUDIO IN and outputs an analog audio output signal ANALOG AUDIO OUT. Although, the illustrated embodiment of DAC 200 is suitable for such applications as digital audio system 100 of FIGURE 1, its utilization is not limited to audio systems, and therefore DAC 200 may be utilized in a range of systems applications requiring the conversion of digital data into analog form.

[0021]   The digital stream AUDIO IN is input into a low voltage current-based
(continuous-time) digital to analog converter (IDAC) 201. The differential outputs of
IDAC 201, after the voltage level shifting discussed further below, drive corresponding
inverting (-) and noninverting (+) low voltage inputs of an operational amplifier stage
202. Operational amplifier 202 also includes differential inverting (-) and non-inverting
(+) outputs, with the noninverting (+) output of operational amplifier 202 driving analog
output (AOUT) pad 203 through resistor 204.

[0022]   Operational amplifier 202 operates around an input common mode voltage
of approximately one (1) volt. The common mode output voltage for operational
amplifier 202 is approximately 4 volts and is controlled by common mode amplifier 205.
The voltage at the inverting (-) input to common mode amplifier 205 is set by a voltage
divider formed by resistors 206 and 207 bridging the noninverting (+) and inverting (-)
outputs of operational amplifier 202. The noninverting (+) input to common mode
amplifier 205 is tied to the common mode voltage (VCM) reference pad 208.

[0023]   Differential operational amplifier 202 is associated with two feedback
loops, one, which couples the inverting (-) input and the noninverting (+) output of
operational amplifier 202, includes a feedback resistor 209a and a feedback capacitor
210a. The second feedback loop, which couples the noninverting (+) input and the
inverting (-) output of operational amplifier 202, includes a feedback resistor 209b and a
feedback capacitor 210b. A level shift generator 211 ensures that an approximately
three (3) volt voltage drop exists across resistors 209a and 209b such that the inputs to
operational amplifier 202 remain within a safe operating voltage range, since low
voltage differential input transistors are utilized in operational amplifier 202 to save chip
area. Generally, a low voltage n-type metal oxide semiconductor [NMOS] transistor has
a channel length approximately eight or nine times shorter than that of a high voltage
NMOS transistor. Additionally, low voltage MOS transistors typically help reduce total
harmonic distortion, since the gate voltage swing is lower, and have better overall noise

performance.

[0024]   A clamp transistor 212 at analog output (AOUT) pad 203 clamps the voltage at output pad 203, in response to the control signal CLAMP, to reduce glitches when powering - up opamp 202. The remaining external load presented to analog output (AOUT) pad 203 is represented in FIGURE 2 by filtering resistors 214 and 215 and a filtering capacitor 216.

[0025]   Isolation transistors 217c and 217d under the control of regulated gate drive 218 respectively isolate the inverting (-) and noninverting (+) inputs of operational amplifier 202 from output pad (AOUT) 203 during the power down operations. Specifically, isolation transistors 217c and 217d prevent current flow from external AC coupling cap 213 and thereby prevent the generation of a large voltage spike, and consequently an audible pop, in the signal ANALOG AUDIO OUT. Pulldown transistors 217a and 217b, also under the control of regulated gate drive 218, respectively pull the inverting (-) and noninverting (+) inputs of operational amplifier 202 to a known voltage, in the illustrated embodiment to ground, after isolation transistors 217c and 217d turn-off.

[0026]   Common mode reference generator 219 generates a common mode reference voltage at VCM pad 208 and the noninverting (+) input of common mode amplifier 205. Common mode reference generator 219 powers down after operational amplifier 202. During power-down, currents through output (AOUT) pad 203 and VCM pad 208 are controlled by ramp down current generator 220 of FIGURE 2.

[0027]   Returning to FIGURE 2, power down of IDAC 202 is controlled by the control SIGNAL POWER DOWN IDAC as delayed by delay 222. The control signal POWER DOWN REFERENCE, as delayed through delay 223, controls power-down of bandgap reference 224, which provides the bias currents to IDAC 201 and operational amplifier 202. Level shifters 225 and 226 shift the low level control signals DRIVER POWER DOWN\ and POWER DOWN VCM\, generated from a low voltage power supply, to the higher levels

required by the circuitry of VCM generator 219 and regulated gate drive 218. To prevent pops in the audio output, the outputs of level shifters 226 and 225 go to a known state and shutdown operational amplifier 202, if the low voltage supply is removed before the high voltage supply.

[0028]   FIGURE 3A is a block diagram showing an N-element embodiment of IDAC array 201 of FIGURE 2. In the illustrated embodiment, complementary input data streams DIN and DINB from the quantizer of a delta-sigma modulator are shifted through a set of one-bit shift register (SR) elements 301a, ..., 301N by the master clock signal MCK, in which N is an integer index. The output of each shift register element 301a, ..., 301N drives a corresponding DAC element 301a, ..., 301N. The resulting overlapping analog output signals drive signal lines INN and INP to the summing nodes at the inputs of opamp 202 of FIGURE 2.

[0029]   A second set of dummy one-bit shift register elements 303a, ..., 303N shift complementary dummy input data streams DIND and DINDB in response to the MCK signal. FIGURE 3B illustrates a selected number of cycles of the MCK, DIN and DIND signals for an embodiment where N is equal to eight. Dummy data streams DIND and DINB are generated relative to the input data streams DIN and DINB such that for every rising edge of the MCK signal, a corresponding edge (rising or falling) occurs on either input data stream DIN or dummy data stream DIND. The outputs from shift register elements 303a, ..., 303N drive a corresponding set of dummy conversion elements 304a, ..., 304N coupled to signal lines INN and INP. Each dummy conversion element 304a, ..., 304N has a capacitance matched to the capacitance of a corresponding DAC element 302a, ..., 302N.

[0030]   FIGURE 4A shows one exemplary current DAC element 302a, ..., N from IDAC array 201 of FIGURES 2 and 3A, along with a more detailed electrical schematic diagram of level shifter 211 of FIGURE 2.

[0031]   The exemplary current element depicted in FIGURE 4A includes a pair of

low voltage PMOS transistors 401a and 401b respectively biased by the bias voltages VBP and VBPC. In the illustrated embodiment, low voltage PMOS transistors 401a and 401b are formed in an isolated well of n-type semiconductor (N-well), to minimize substrate noise coupling into IDAC 201, and save chip area. The current through PMOS transistors 401a and 401b from the voltage rail Vdda feed the current paths of NMOS transistors 402a and 402b. The gates of NMOS transistors 402a - 402b are respectively driven by corresponding complementary digital data input bits DIN_x and $DINB_x$ from the outputs of the corresponding shift register element 301a,..., N of FIGURE 3A, in which x is an integer index from 0 to N. The sources of NMOS transistors 402a and 402b are coupled to the outputs INN and INP of IDAC 201 of FIGURE 2. The remaining DAC elements 302a, ..., N of IDAC 201 (not shown) are similarly configured and similarly coupled to the outputs INN and INP, which are in turn connected to the inverting (-) and non-inverting (+) summing nodes of operational amplifier 202 of FIGURE 2.

[0032]   The voltage level shifting operations of voltage level generator 211, discussed above in conjunction with FIGURE 2, are implemented by a pair of identical NMOS current source transistors 403a and 403b, biased by the bias voltage VBN. The current through NMOS current source transistors 403a and 403b is set, in the illustrated embodiment, to produce a voltage drop of approximately three (3) volts across operational amplifier feedback transistors 209a and 209b of FIGURE 2. Any noise in the bias signal VBN is advantageously attenuated by the internal common mode feedback loop within operational amplifier 202.

[0033]   Current source transistors 403a and 403b operate in conjunction with a pair of NMOS cascode transistors 404a and 404b, biased by the bias voltage VBNC, and a chopper circuit 405. Chopper circuit 405 includes a pair of NMOS transistors 406a and 406b switching in response to the control signal CHOP and a pair of NMOS transistors 407a and 407b operating in response to the complementary control signal

CHOPB.

[0034]   FIGURE 4B illustrates one exemplary circuit suitable for generating the non-overlapping control signals CHOP and CHOPB. In the illustrated embodiment of FIGURE 4B, the chopping control signal CHOP and CHOPB are generated from a high frequency clock CHOP_CLK which is generated from the clock driving the digital data being converted. The circuitry of FIGURE 4B includes an input inverter 408, a pair of cross-coupled NAND gates 409a and 409b, and a set of inverter/ drivers 410a- 410d.

[0035]   Current source transistors 403a and 403b of FIGURE 4A generate intrinsic low frequency flicker (1/F) noise, which generally has a power spectral density which is inversely proportional to frequency. According to the principles of the present invention, chopping circuitry 405 chops the NMOS current source transistors 403a and 403b at a high frequency and therefore shifts (modulates) the flicker noise spectrum to much higher out-of-band frequencies. Consequently, the overall noise generated by level shifting circuitry 211 within the signal band of the output signal ANALOG AUDIO OUT of FIGURE 2 is reduced.

[0036]   Each DAC element 302a,..., 302N of FIGURE 3A is associated with a corresponding dummy circuit 411, as shown in Fig. 4A. In the illustrated embodiment, each dummy circuit 411 includes a PMOS transistor 412, with the gate shorted to the source, and a pair of NMOS transistors 413a and 413b, having gates controlled by the complementary data bits DIN_x and $DINB_x$. The sources of NMOS transistors 413a and 413b are respectively coupled to the signal lines INP and INN and cross-coupled to the sources of NMOS transistors 402a and 402b of the corresponding DAC element 302a,..., 302N. The parasitic capacitances at nodes n3 of DAC element 302a,..., 302N and n4 of corresponding dummy circuit 411 of FIGURE 4A are matched.

[0037]   The dummy element 411 associated with each DAC element 302a,..., 302N makes the load on signal lines INN and INP independent of the corresponding input bits DIN_x and $DINB_x$, reduces the instantaneous differential current change ("kick") on

signal lines INN and INP, and improves the power supply rejection ratio (PSRR) on the input bits DIN_x and $DINB_x$. For example, when data bit DIN_x is high and the complementary bit $DINB_x$ is low, the parasitic capacitance at node n3 of exemplary DAC element 302a,..., N of FIGURE 4A is coupled to the INN signal line through transistor 402a while the matched capacitance at node n4 of dummy cell 411 is coupled to the INP signal line through transistor 413a. Consequently, the capacitive load on signal lines INN and INP is independent of the states of DIN_x and $DINB_x$, and the resulting instantaneous differential current change on signal lines INN and INP is reduced. Furthermore, noise associated with the input bits DIN_x and $DINB_x$ is coupled to both signal lines INN and INP by transistors 402a- 402b and 413a- 413b as common mode noise, which is subsequently zeroed – out by the common mode loop internal to opamp 202 of FIGURE 2.

[0038]   FIGURE 5 is an electrical schematic diagram of a representative dummy element 304a,..., 304N shown in FIGURE 3A. Each dummy element 304a,..., 304N includes a pair of PMOS transistors 501a and 501b having gates and sources coupled together and to the supply voltage Vdda. The drain of transistor 501a is coupled to the drains of a pair of NMOS transistors 502a and 502b having gates respectively controlled by the dummy data bits $DIND_x$ and $DINDB_x$ from the corresponding dummy shifter register element 303a,..., 303N of FIGURE 3A. The drain of transistor 501b is coupled to the drains of NMOS transistors 503a and 503b, which have gates respectively controlled by the dummy bits $DINDB_x$ and $DIND_x$. The sources of transistors 502a and 502b are then cross-coupled with the sources of transistors 503a and 503b and the signal lines INN and INP. The parasitic capacitance at nodes n5 and n6 match the capacitance at nodes n3 and n4 of a corresponding DAC element 302a,..., N, of FIGURE 4A.

[0039]   Returning to FIGURE 2, in the illustrated embodiment of digital to analog converter 200, the voltages at the inverting (-) and noninverting (+) inputs of operational amplifier 202 do not completely settle during data conversion operations. Chopping

circuitry 405 of FIGURE 4A is disposed between NMOS current source transistors 403a
and 403b and NMOS cascode transistors 404a and 404b. The gain of cascode
transistors 404a and 404b advantageously reduces the effects of the non - settled
voltage at the inverting and non-inverting inputs of operations amplifier 202 during
charging and discharging of the parasitic capacitance at the chopping nodes n1 and n2
of FIGURE 4A. As a result, the process of chopping the flicker noise generated by
NMOS current source transistors 403a and 403b is independent of the non-settled
voltage at the INN and INP nodes.

[0040]   In the illustrated embodiment, the data bits DIN_x and $DINB_x$ output from
each shift register 301a, ..., 301N of FIGURE 3A overlap to ensure that transistors 402a
and 402b shown in FIGURE 4A for DAC elements 302a, ..., 302N do not simultaneously
turn-off and thereby cause a glitch on the INN and INP data lines and the inputs of opamp
202 of FIGURE 2. Instead, during the overlap period of bits DIN_x and $DINB_x$, both
transistors 402a and 402b turn-on, which results in a short between the sources of
transistors 402a – 402b in FIGURE 4A. Specifically, since the voltages at the inputs to
opamp 202 of FIGURE 2 do not settle completely, the remaining voltage between INN
and INP is sampled onto the parasitic capacitance on nodes n3 and n4. Subsequently,
on the following rising edges of bits DIN_x and $DINB_x$, the high frequency noise stored on
nodes n3 and n4 are mixed through transistors 402a and 402b on to the signal lines INN
and INP, as noise and distortion folding into the audio signal baseband.

[0041]   According to the principles of the present invention, overlapping dummy
bits $DIND_x$ and $DINDB_x$ of FIGURE 5, generated from dummy data streams DIND and
DINDB of FIGURES 3A and 3B, ensure that, for each DAC element 302a, ..., 302N which
does not switch for a given rising edge of the MCK signal, the corresponding dummy
element 304a,..., 304N does switch, and vice - versa. For that dummy element 304a,...,
304N, the parasitic capacitances at nodes n5 and n6, shown in FIGURE 5, are
impressed with the time-dependent signal. During the subsequent transitions of $DIND_x$

and $DINDB_x$, the signal impressed on the capacitances of nodes n5 and n6 are transferred to the INN and INP signal lines through transistors 503a – 503b and 502a – 502b, depending on the polarity of $DIND_x$ and $DINDB_x$. During the overlap period of bits $DIND_x$ and $DINDB_x$, both transistors 502a-502b turn on, which results in a short between the sources of transistors 502a-502b. This results in a charge transfer between INN and INP data lines.

[0042]　　　Overall, the total contribution of noise and distortion on signal lines INN and INP becomes dependent on the MCK signal rather than on the data signals DIN and DINB. In the illustrated embodiment, the noise transfer function of delta – sigma modulator 305 is then designed to have a minimum noise floor with respect to the known frequency of the MCK signal such that the mixing of high frequencies on the signal lines is more controlled and the fold back of noise into the signal baseband can be minimized.

[0043]　　　While a particular embodiment of the invention has been shown and described, changes and modifications may be made therein without departing from the invention in its broader aspects, and, therefore, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of the invention.